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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of: Andreas C. DOERING

Serial No.: 10/696,865

Filed: October 30, 2003

Date: February 13, 2008

Confirmation No.: 8071

Group Art Unit: 2183

Examiner: Brian P. Johnson

For: SYSTEM FOR USING FPGA TECHNOLOGY WITH A MICROPROCESSOR FOR RECONFIGURABLE, INSTRUCTION LEVEL HARDWARE ACCELERATION

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT UNDER 37 C.F.R. §1.312

Sir:

Please amend the above-identified application in the following manner.

Amendment to the Specification which begins on page 2 of this paper.

Remarks/Arguments begin on page 3 of this paper.